

**IN THE CLAIMS:**

Amend claims 1-8, 10-13 and 17 as shown in the following listing of claims, which replaces all previous listings and versions of claims.

1. (currently amended) A voltage detecting circuit, comprising:

a first terminal connected to a positive pole of a battery;

a second terminal connected to a negative pole of the battery;

a voltage dividing circuit that divides a voltage across the battery;

a reference voltage circuit that generates a reference voltage;

a comparator that compares outputs of the reference voltage circuit and the voltage dividing circuit and outputs a comparison signal;

a first output circuit connected between the first terminal and the second terminal for outputting a first output signal on the basis of the comparison signal output by the comparator;

an output terminal for outputting the first output signal; and

a second output circuit connected between the output terminal and one of the first and second terminals for outputting a second output signal that changes in value on the basis of a first signal and a second signal at the first terminal and the second terminal, respectively.

~~a second output circuit for outputting a second output signal that changes in value based on a voltage of the battery and on the basis of signals at the first terminal and the second terminal; and~~

~~an output terminal for outputting the first and second output signals.~~

2. (currently amended) A voltage detecting circuit according to claim 1; wherein the second output circuit comprises a depletion-type ~~n-ch~~ n-channel MOS transistor and a depletion-type ~~p-ch~~ p-channel MOS transistor connected in series between the output terminal and one of the first terminal and the second terminal; and wherein a the first ~~signal based on a voltage of~~ at the first terminal is input to a gate electrode of the depletion-type ~~p-ch~~ p-channel MOS transistor, and a the second ~~signal based on a voltage of~~ at the second terminal is input to a gate electrode of the depletion-type ~~n-ch~~ n-channel MOS transistor.

3. (currently amended) A voltage detecting circuit according to claim 2; wherein the first output circuit comprises an enhancement-type ~~n-ch~~ n-channel MOS transistor and an enhancement-type ~~p-ch~~ p-channel MOS transistor connected in series between the first terminal and the second terminal; and wherein a signal based on the comparison signal output by the comparator is input to gate electrodes of the enhancement-type ~~p-ch~~ p-channel MOS transistor and the enhancement-type ~~n-ch~~ n-channel MOS transistor, and absolute values of threshold voltages of the depletion-type ~~n-ch~~ n-channel MOS transistor and the depletion-type ~~p-ch~~ p-channel MOS transistor are larger than absolute values of threshold voltages of the enhancement-type ~~n-ch~~ n-channel MOS transistor and the enhancement-type ~~p-ch~~ p-channel MOS transistor.

4. (currently amended) A voltage detecting circuit according to claim 2; wherein the first terminal is connected to a the gate electrode of the depletion-type ~~p-ch~~ p-channel MOS transistor and the second terminal is connected to a the gate electrode of the depletion-type ~~n-ch~~ n-channel MOS transistor.

5. (currently amended) A voltage detecting circuit according to claim 3; wherein the comparison signal is input to gate electrodes of the enhancement-type ~~p-ch~~ p-channel MOS

transistor and the enhancement-type ~~n-ch~~ n-channel MOS transistor.

6. (currently amended) A voltage detecting circuit according to claim 1; wherein the first output circuit comprises two enhancement mode MOS transistors connected in series between the ~~input~~ first and second terminals.

7. (currently amended) A voltage detecting circuit according to claim 6; wherein the second output circuit comprises two depletion mode MOS transistors connected in series between the output terminal and one of the ~~input~~ first and second terminals.

8. (currently amended) A voltage detecting circuit, comprising: input terminals; an output terminal; a reference voltage generator for generating a reference voltage; a comparator for comparing a voltage across the input terminals with the reference voltage and outputting a comparison signal; a first output circuit connected between the input terminals for outputting a first signal to the output terminal on the basis of the comparison signal; and a second output circuit ~~for outputting a second signal to the output terminal which changes in level based on the signal on the input terminals~~ connected between the output terminal and one of the input terminals for varying a resistance value between the output

terminal and one of the input terminals based on the voltage across the input terminals.

9. (previously presented) A voltage detecting circuit according to claim 8; wherein the input terminals comprise a pair of terminals connected to opposite poles of a battery.

10. (currently amended) A voltage detecting circuit according to claim 6 8; further comprising a voltage dividing circuit for dividing a voltage across the input terminals and outputting a divided voltage to the comparator.

11. (currently amended) A voltage detecting circuit according to claim 6 8; wherein the first output circuit comprises two enhancement mode MOS transistors connected in series between the input terminals.

12. (currently amended) A voltage detecting circuit according to claim 6 11; wherein the two enhancement mode MOS transistors have opposite polarities.

13. (currently amended) A voltage detecting circuit according to claim 12; wherein an output of the comparator is connected to gate electrodes of the two enhancement mode MOS transistors.

14. (previously presented) A voltage detecting circuit according to claim 13; wherein the second output circuit comprises two depletion mode MOS transistors connected in series between the output terminal and one of the input terminals.

15. (previously presented) A voltage detecting circuit according to claim 14; wherein the two depletion mode MOS transistors have opposite polarities.

16. (previously presented) A voltage detecting circuit according to claim 15; wherein a gate electrode of one of the depletion mode MOS transistors is connected to one of the input terminals, and a gate electrode of the other depletion mode MOS transistor is connected to another one of the input terminals.

17. (currently amended) A voltage detecting circuit according to claim 16; wherein absolute values of threshold ~~voltage~~ voltages of the depletion mode MOS transistors are larger than absolute values of threshold voltages of the enhancement mode MOS transistors.